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WHAT IS CLAIMED IS:

1. A pipeline structure for use in a digital system, said pipeline structure comprising:

a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least one intermediate stage being interposed between the first stage and the last stage; and

a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage,

wherein the first stage and the last stage are controlled by a main clock signal,

the at least one local clock signal is generated from the main clock signal, and

the main clock signal and the at least one local clock signal are out of phase.

2. The pipeline structure according to claim 1,

wherein the at least one intermediate stage consists of a plurality of intermediate stages,

each of the intermediate stages is controlled by a corresponding local clock signal that is generated by the phase shifting circuit, and

the local clock signals are all out of phase with one another.

3. The pipeline structure according to claim 2, wherein for each of the intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence.

4. The pipeline structure according to claim 3, wherein each of the delay blocks produces the local clock signal for controlling the corresponding intermediate stage from the clock signal controlling a next one of the stages in the sequence.

5. The pipeline structure according to claim 4, wherein each of the intermediate stages includes a functional unit cascade connected to a buffer, the buffer storing an output of the functional unit of a previous one of the stages in the sequence based on the corresponding local clock signal, and the functional unit having a propagation time that is less than a phase difference between the corresponding local clock signal and the clock signal controlling the next one of the stages in the sequence.

6. The pipeline structure according to claim 5, wherein each of the functional units consists of a combinatorial circuit and each of the buffers consists of a register for storing a word.

7. The pipeline structure according to claim 1, wherein for each of the at least one intermediate stages, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence.

8. A digital system including at least one pipeline structure, the pipeline structure comprising:

a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least one intermediate stage being interposed between the first stage and the last stage; and

a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage,

wherein the first stage and the last stage are controlled by a main clock signal,

the at least one local clock signal is generated from the main clock signal, and

the main clock signal and the at least one local clock signal are out of phase.

9. The digital system according to claim 8,

wherein the at least one intermediate stage of the pipeline structure consists of a plurality of intermediate stages,

each of the intermediate stages is controlled by a corresponding local clock signal that is generated by the phase shifting circuit, and

the local clock signals are all out of phase with one another.

10. The digital system according to claim 9, wherein for each of the intermediate stages of the pipeline structure, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence.

11. The digital system according to claim 10, wherein each of the delay blocks produces the local clock signal for controlling the corresponding intermediate stage from the clock signal controlling a next one of the stages in the sequence.

12. The digital system according to claim 8, wherein the digital system is a synchronous digital system.

13. The digital system according to claim 8, wherein the digital system is a controller or microprocessor integrated in a chip.

14. An electronic device comprising:

a digital system including at least one pipeline structure, the pipeline structure including:

a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least one intermediate stage being interposed between the first stage and the last stage, and the first stage and the last stage being controlled by a main clock signal; and

a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage, the at least one local clock signal being generated from the main clock signal, and the main clock signal and the at least one local clock signal being out of phase; and

a battery for supplying the digital system.

15. The electronic device according to claim 14,

wherein the at least one intermediate stage of the pipeline structure of the digital system consists of a plurality of intermediate stages,

each of the intermediate stages is controlled by a corresponding local clock signal that is generated by the phase shifting circuit, and

the local clock signals are all out of phase with one another.

16. The electronic device according to claim 15, wherein for each of the intermediate stages of the pipeline structure of the digital system, the phase shifting circuit includes a delay block for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence.

17. The electronic device according to claim 16, wherein each of the delay blocks produces the local clock signal for controlling the corresponding intermediate stage from the clock signal controlling a next one of the stages in the sequence.

18. The electronic device according to claim 14, wherein the electronic device is a hand-held computer and the digital system is a controller or microprocessor of the hand-held computer.

19. A method of operating a pipeline structure that includes a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least one intermediate stage being interposed between the first stage and the last stage, said method comprising the steps of:

controlling the first stage and the last stage with a main clock signal;

generating at least one local clock signal from the main clock signal, the main clock signal and the at least one local clock signal being out of phase; and

controlling the at least one intermediate stage with the at least one local clock signal.

20. The method according to claim 19,

wherein the at least one intermediate stage consists of a plurality of intermediate stages,

in the generating step, one local clock signal is generated for each of the intermediate stages,

in the controlling step, each of the intermediate stages is controlled by a corresponding one of the local clock signals

21. The method according to claim 20, wherein the local clock signals are all out of phase with one another.

22. The method according to claim 20, wherein in the generating step, the local clock signal for each of the intermediate stages is generated from the clock signal controlling one of the stages that is adjacent in the sequence.

23. The method according to claim 22, wherein in the generating step, the local clock signal for each of the intermediate stages is generated from the clock signal controlling a next one of the stages in the sequence.